REMARKS

The Office Action dated April 21, 2004 has been received and carefully considered. In this response, claims 1, 4, 6, 7-10, 13, 14 and 21 have been amended to improve their form and readability. The amendments to the claims do not narrow the scope of the claims and have not been provided for purposes of patentability. Support for the amendments to the claims may be found in the specification and figures as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Allowability of Claim 7

The Applicants note with appreciation the indication at page 7 that claim 7 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In the interest of advancing the present application, the Applicants have rewritten claim 7 pursuant to the Examiner's comments. Withdrawal of the objection to claim 7 therefore is respectfully requested.

Indefinite Rejection of Claim 17

At page 2 of the Office Action, claim 17 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is respectfully traversed.

Claim 17 recites a multiplexor having a control input coupled to an output of a first register, a first data input coupled to the address control pin, a second data input coupled to a first data lane enable, and an output coupled to an output pin. With respect to this claim, the Examiner asserts that the function of this multiplexor is not understood since it seems that the system would operate effectively without it. The Applicants respectfully disagree. As one of ordinary skill in the art would realize from the context of claim 17 (and claim 16 from which claim 17 depends), the multiplexor in question functions so as to select one of its two data inputs (i.e., the address control pin and the first data lane enable) for output to the output pin, where the output of the first register is used to select between the two data inputs. Regardless of whether the "system would operate effectively without [the multiplexor]," the purpose of claim 17 is to more particularly point out and distinctly claim an additional feature of the apparatus of claim 16. Accordingly, it is respectfully submitted that claim 17 is proper and withdrawal of this

rejection therefore is respectfully requested.

Anticipation Rejection of Claims 1-5, 8-10, 16, 18, 19 and 21

At page 3 of the Office Action, claims 1-5, 8-10, 16, 18, 19 and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Chang (U.S. Patent Application Publication No. 2003/0005247). This rejection is respectfully traversed.

Claim 1, from which claims 2-6 and 8-10 depend, recites, in part, the limitations of, when in a first mode of operation, *utilizing a first output to provide a first data lane enable* for facilitating access of a portion of a first memory storage location associated with a first memory address, and, when in a second mode of operating, *utilizing the first output to provide an address bit* of a second memory address for facilitating designation of a second memory storage location. To paraphrase, claim 1 recites the limitations wherein a first output is used to provide either a first data lane enable or an address bit, depending on the mode of operation. Claims 19 and 21 recite similar limitations. Claim 16 recites, in part, the limitations of an output pin coupled to both the output of an address control portion and an output of a data lane enable control portion.

With respect to these limitation of claims 1, 19 and 21, the Examiner asserts that Chang discloses "utilizing a first output (Figure 3, Software Interrupt from 100) to provide a first data lane enable (SMI Signal) for facilitating access of a portion of a first memory storage location . . ., and when in a second mode of operation utilizing the first output for facilitating designation of a second memory storage location." Office Action, p. 3. However, the Examiner fails to cite a particular passage of Chang which discloses or suggests the use of a single output to provide either a data lane enable or an address bit, depending on mode of operation, as recited in claims 1, 19 and 21. The Applicants respectfully submit that Chang fails to disclose or even suggest at least these limitations. As noted at paragraphs 0033 and 0039 and Figure 2 of Chang, Chang teaches the provision of an SMI signal (which the Examiner appears to equate to the first data lane enable of the claims) via an SMIOUT# pin. Thus, in the context of the Examiner's assertions, the SMIOUT# pin would be considered equivalent to the first output of claims 1, 19 and 21. However, contrary to claims 1, 19 and 21, Chang fails to disclose or suggest the provision of any portion of an address via the same output used to provide the data lane enable (i.e., the SMIOUT# pin of Chang) when in a different mode of operation. In fact, Chang teaches the provision of the SMI signal *from the chip set 220* to the CPU 200 and the provision of the

memory address *from the CPU 220*. Thus, not only does Chang fail to teach using a single port to provide either of a data lane enable or an address bit, Chang teaches away from the limitations of claims 1, 19 and 21 by disclosing the provision of the SMI signal and the memory address *via separate components*. *Chang*, paragraph 0031. *See also Chang*, paragraph 0033 (disclosing that the "chipset [220] can arise a system management (SMI) signal (an enable signal from the SMIOUT# pin) triggering the CPU in to the SMM 180. In the SMM 180, the SMI handler routine is able to access the memory space . . . ."). Thus, Chang fails to disclose or even suggest each and every limitation of claims 1, 19 and 21 as well as claims 1-6, 8-10 and 20 at least by virtue of their dependency from one of claims 1 or 19. Moreover these claims recite additional limitations not anticipated by Chang or obvious in view of Chang.

With respect to claim 16, the Examiner asserts that Figure 3 discloses the limitations of an output pin coupled to the output of an address control portion (which the Examiner appears to equate to element 160 of Figure 3 of Chang) and an output of the first data lane enable control portion (which the Examiner appears to equate to the SMI signal of Chang). However, the Applicants respectfully disagree and submit that Chang fails to disclose or suggest output pin coupled to both the output of the address control portion and the output of the data lane enable control portion as recited in claim 16. As noted above, Chang teaches the provision of the SMI signal and the memory address via separate components (i.e., via the chipset 220 and the CPU 200, respectively). Neither Figure 3 nor the corresponding passages of Chang disclose or suggest a single output pin coupled to the outputs of both the chipset 220 and the CPU 200 in any way. Accordingly, Chang fails to disclose or even suggest each and every limitation of claim 16 and therefore fails to disclose each and every limitation of claim 18 at least by virtue of its dependency from claim 16.

Accordingly, it is respectfully submitted that the anticipation rejection of claims 1-5, 8-10, 16, 18, 19 and 21 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 4, 12 and 19

At page 4 of the Office Action, claims 6, 11-15 and 20 were rejected under 35 U.S.C § 103(a) as being unpatentable over Chang. This rejection is respectfully traversed.

Claim 6 depends from claim 1 and claim 20 depends from claim 19. As noted above, Chang fails to disclose or suggest the limitations of a single output to provide either a data lane enable or an address bit based on a mode of operation as recited in claims 1 and 19. Chang therefore fails to disclose each and every limitation of claims 6 and 20 at least by virtue of their dependency on one of claims 1 and 19.

Claim 11, from which claims 12-14 depend, recites, in part, the similar limitations of: during a first mode of operation, multiplexing a first set of data onto a set of pins of a device to provide data representing two least significant bits of a first address, a most significant bit of the first address and a lane enable; during a second mode of operation, multiplexing a second set of data onto the set of pins to allow the set of pins to provide data representing one least significant bit of a second address, a most significant bit of the second address, and two lane enables; and, during a third mode of operation, multiplexing a third set of data onto the set of pins to allow the set of pins to provide four lane enables. Claim 15 recites, in part, the related limitations of: a first output node to provide one of an address data for address location A(1) and a data lane enable based upon a mode of operation; a second output node to provide on of an address data for address location A(0) and a data lane enable signal based upon the mode of operation; and a third output node to provide one of an address data for address location A(n+1) and a data lane enable signal based upon the mode of operation.

With regard to these limitations, the Examiner asserts that "[i]t is understood that 'data lane' enable information is simply any signal that can be used to indicate what portion of data is to be accessed" and therefore concludes that "any signal being used by the system of Chang to access the various addressing ranges can in fact be a data lane signal." Office Action, p. 5. The Examiner further suggests, in view of this overly broad interpretation, that a data lane enable can comprise memory address bits that are used in the facilitation of access to a particular memory location. As a first matter, the Applicants respectfully submit that the Examiner's extremely broad interpretation of a data lane enable is inconsistent with the context of the claims and the teachings of the specification. As taught by the present application, a lane enable describes

> a signal that is used to indicate a portion of a data word or partial data that is to be accessed. The lane enable can function as a strobe, or clocking-type signal, to provide a timing event to indicate when a portion of the data can be accessed. For example, a lane enable can function as a byte lane strobe during a write to

> memory, whereby a timing event, such as a rising edge, indicates when a portion of the data word can be written to memory. In another application, the lane enable does not provide any timing events, but instead is used to enable specific data portions to be access to and from a memory component or system.

Present Application, p. 3, line 19 to p. 4, line 2.

Thus, contrary to the Examiner's assertions, a data lane enable is not "simply any signal that can be used to indicate what portion of data is to be accessed" but is instead a signal, such as a timing event or strobe, used to indicate which portion of a data word is to be accessed. As will be understood by one of ordinary skill in the art, memory addresses typically are word-aligned, i.e., accessible by data word only. Thus, to assert that memory address bits can act as a data lane enable to access only a portion of a data word is contrary to this conventional arrangement. As a second issue, the Office Action has failed to establish that Chang discloses or suggests the multiplexing of any data onto any sets of pins, much less multiplexing the specified sets of data as recited in claim 11. To demonstrate, the Office Action fails to discuss how Chang discloses the least significant bit, most significant bit and data lane enable limitations recited in claim 11. Furthermore, the Office Action has failed to establish that Chang discloses a set of pins having the combinations of least significant bits and the most significant bit of an address and the one or more lane enables as recited in claim 11. In addition, the Office Action has failed to establish that Chang discloses or suggests multiple output nodes, each having the different specified combinations of address data of an address location and a data lane enable signal as recited in claim 15. Accordingly, it is respectfully submitted that the Office Action fails to establish that Chang discloses each and every limitation of claims 11 and 15 and further fails to establish that Chang discloses each and every limitation of claims 12-15 at least by virtue of their dependency on claim 11.

Accordingly, it is respectfully submitted that the obviousness rejection of claims 11-15 and 20 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Conclusion

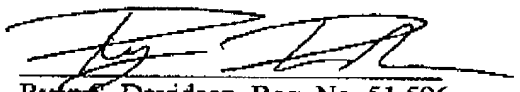
In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The

Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

June 21, 2004
Date



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